Universal Logic Circuits

Description

The UG series of ULC™s is well suited for conversion of medium- to-large sized CPLDs and FPGAs. Devices are implemented in high-performance CMOS technology with 0.6-mm (drawn) channel lengths, and are capable of supporting flip-flop toggle rates of 350 MHz, operating clock frequencies up to 150 MHz and input to output delays as fast as 5 ns.

The architecture of the UG series allows for efficient for conversion of many PLD architecture and FPGA device types. A compact RAM cell, along with the large number of available gates allows the implementation of RAM in FPGA architectures that support this feature, as well as JTAG boundary-scan and scan-path testing.

Conversion to the UG series of ULC can provide a significant reduction in operating power when compared to the original PLD or FPGA. This is especially true when compared to many PLD and CPLD architecture devices, which typically consume 100 mA or more even when not being clocked. The UG series has a very low standby consumption of 0.4 nA/gate typically, which would yield a standby current of 4 mA on a 10,000 gate design. Operating consumption is a strict function of clock frequency, which typically results in a power reduction of 50% to 90% depending on the device being compared.

The UG series provides several options for output buffers, including a variety of drive levels up to 24 mA. Schmitt trigger inputs are also an option. A number of techniques are used for improved noise immunity and reduced EMC emissions, including: several independent power supply busses and internal decoupling for isolation; slew rate limited outputs are also available as required.

The UG series is designed to allow conversions of high performance 3-V devices as well as 5-V devices. Support of mixed supply conversions is also possible, allowing optimal trade-offs between speed and power consumption.

Features

- High performance ULC family suitable for medium- to large-sized CPLDs and FPGAs
- Conversions to over 200,000 FPGA gates
- Pin counts to over 300 pins
- Any pin-out matched due to limited number of dedicated pads
- Advanced 0.6-mm (drawn)/0.45-mm (effective) feature size
- Triple-layer or dual-layer metal CMOS technology
- High speed performance:
  - 250-ps typical cell delay
  - 350-MHz toggle rate
- Full range of packages: DIP, SOIC, LCC/PLCC, PQFP/TQFP, PGA/PPGA
- 3-V to 5-V operation.
- Low quiescent current: 0.4 nA/gate
- Available in commercial, industrial, automotive, military and space grades.

Product Outline

Part Number	Pads	Equivalent FPGA Gates	Maximum Drive
UG00	24	1800	N/A
UG01	32	3300	N/A
UG02	36	4200	180
UG04	48	7500	310
UG09	72	15800	790
UG14	88	24300	1210
UG20	104	34800	1740
UG33	130	46000	2880

Part Number	Pads	Equivalent FPGA Gates	Maximum Drive
UG42	146	58600	3660
UG52	162	63700	4550
UG70	188	85800	6130
UG90	212	108500	7750
UG120	244	145100	10360
UG140	264	156800	12250
UG200	312	206300	17190

Architecture

The basic element of the UG family is called a cell. One cell can typically implement between two to three FPGA gates. Cells are located contiguously through- out the core of the device, with routing resources provided in two or three metal layers above the cells. Some cell blockage does occur due to routing, and utilization will be significantly greater with three metal routing than two. The sizes listed in the Product Outline are estimated usable amounts using three metal layers. I/O cells are provided at each pad, and may be configured as inputs, outputs, I/Os, V_{DD} or V_{SS} as required to match any FPGA or PLD pinout. Special function cells and pins are located in the corners which typically are unused.

The “Max Bits RAM” column listed in the Product Outline table details the maximum amount of Xilinx XC4000 style RAM (16 x 1 blocks etc.) that could be implemented in each matrix if all of the cells were used for RAM. In an actual circuit, some of the cells would be required to implement logic, so the actual amount of RAM would need to be reduced to accommodate the logic.

In order to improve noise immunity within the device, separate V_{DD} and V_{SS} busses are provided for the internal cells and the I/O cells.

I/O Options

Inputs

Each input can be programmed as TTL, CMOS, or Schmitt Trigger, with or without a pull up or pull down resistor.

Fast Output Buffer

Fast output buffers are able to source or sink 3 to 12 mA according to the chosen option.

Slew Rate Controlled Output Buffer

In this mode, the p- and n-output transistor commands are delayed, so that they are never “ON” together, resulting in a low switching current and low noise. These buffer are dedicated to very high load drive.

3.3-V Compatibility

The UG series of ULCs is fully capable of supporting high-performance operation at 3.3 V or 5 V. The performance specifications of any given ULC design however, must be explicitly specified as 3.3 V, 5 V or both.

Power Supply and Noise Protection

In order to improve the noise immunity of the UG series, several mechanisms have been implemented inside the UG devices. Two kinds of protection have been added: one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the core.

I/O buffers switching protection

Three features are implemented to limit the noise generated by the switching current: The power supplies of the input and output buffer are separated. The rise and fall times of the output buffers can be controlled. The number of buffers that are connected on the same power supply line is limited.

Core switching current protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added: Some decoupling capacitors are integrated directly on the silicon to reduce the power supply drop. A power supply network has been implemented in the matrix. This solution lessens the parasitic elements such as inductance and resistance and constitutes an artificial V_{DD} and V_{SS} plane. One mesh of the network supplies approximately 150 cells. A low-pass filter has been added between the core and the inputs of the output buffers. This limits the transmission of the noise coming from the ground or the V_{DD} supply of the core via the output buffers.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . –0.5 V to 7.0 V
Input Voltage (V_{IN}) . . . . . –0.5 V to V_{DD} + 7.0 V
Storage Temperature . . . . . –65 to 150°C

Recommended Operating Range

V_{DD} . . . . . 5 V ±5% or 3.3 V ±5%
Operating Temperature
Commercial . . . . . 0 to 70°C
Industrial . . . . . –40 to 85°C
Military . . . . . –55 to 125°C

DC Characteristics

Parameter	Symbol	Base Part T_A = Commercial	Min	Typ	Max	Unit
Output Voltage	V_{OH}	I_{OH} = 24, 12, 6, 3 depending on buffer	2.4			V
	V_{OL}	I_{OL} = –24, –12, –6, –3 depending on buffer			0.4	
Input Voltage	V_{IH}		2.0			
	V_{IL}				0.8	
Input Leakage Current	I_{IX}	$V_{IN} = V_{SS}$	–5	–1		mA
		$V_{IN} = V_{DD}$		1	5	
		$V_{IN} = V_{SS}$, with pull-up	–100	–40		
		$V_{IN} = V_{DD}$, with pull-down		40	100	
Output Leakage Current	I_{OZ}	$V_{OUT} = V_{SS}$ or V_{DD}	–5	±1	5	
Output Short Circuit Current	I_{OS}	$V_{OUT} = V_{DD}$		90	160	mA
		$V_{OUT} = V_{SS}$	–130	–60		
Standby Current	I_{CCSB}	V_{DD} = 5.25 V, $V_{IN} = V_{SS}$		0.4	1	nA/Gate
Operating Current	I_{DDOP}			0.3	0.4	mA/Gate/ MHz
Input Capacitance	C_{IN}	V_{DD} = 5.0 V, V_{IN} = 2.0 V		2.5		pF
Output Capacitance	C_{OUT}	V_{OUT} = 2.0 V		2		

Notes
a. I_{OH} = 24, 12, 6,3. Selection determined by FPGA or PLD data sheet requirements.

Internal Timing Characteristics

These timing parameters for selected macro cells are provided for information only. Only pin-to-pin timing characteristics are guaranteed for ULCs, and the actual specification is determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed to separately by MHS.

Conditions: V_{DD} = 5 V, Typical Process, Statistical Wire Length. All delays measured at V_{IN}/V_{OUT} = 2.5 V.

Macro Type		Parameter	Symbol	Min	Max[a]	Max[b]	Units
2-Input NAND	NAND2				0.39	0.56	
4-Input NAND	NAND4	Propagation Time	t_{PD}		0.68	0.88	ns
Inverter	INV				0.41	0.68	
Inverting Tri-State Buffer	TRISTAN				0.74	0.99	
		Enable Time	t_{EN}		0.69	0.97	

Internal Timing Characteristics (Cont'd)

Macro Type		Parameter	Symbol	Min	Max[a]	Max[b]	Units
Resetable Latch	LATCHR	Setup Time	t_{SU}	0.60			ns
		Hold Time	t_H	0.00			
		Pulse Width	t_{PW}				
		Propagation Time	t_{DQ}		0.97	1.25	
		Enable Time	t_{EN}		1.22	1.49	
		Reset Time	t_{RN}		0.87	1.10	
D Flip-Flop with Reset	FDFFR	Setup Time	t_{SU}	0.40			
		Hold Time	t_H	0.00			
		Pulse Width	t_{PW}	0.60			
		Clock Delay Time	t_{CQ}		0.95	1.22	
		Reset Time	t_{RN}		0.81	0.94	
TTL Compatible Input Buffer	BUFINTTL	Propagation Time	t_{PLH}		0.80	0.95	
			t_{PHL}		0.68	0.74	
TTL Compatible I/O Buffer Input Mode	BIOT12		t_{PLH}		0.80	0.95	
			t_{PHL}		0.68	0.74	
Output Buffer	BOUT6		t_{PLH}		2.97	8.18	
			t_{PHL}		1.96	4.23	
TTL Compatible I/O Buffer	BIOT12		t_{PLH}		2.49	6.42	
			t_{PLH}		1.74	3.47	
		Enable Time	t_{PZH}		3.27	7.17	
			t_{PZL}		1.60	3.30	
Tri-State Output Buffer	B3STA12	Propagation Time	t_{PLH}		2.49	6.42	
			t_{PHL}		1.74	3.47	
		Enable Time	t_{PZH}		3.27	7.17	
			t_{PZL}		1.60	3.30	

Notes
a. Fan-outs are three internal loads for NAND2 and NAND4, four loads for all other internal macros and input buffers. Loading of B_{OUT6} is 20 pF, BIOT12 and B3STA12 are 30 pF.
b. Fan-outs are six internal loads for NAND2, seven loads for NAND4, nine loads for all other internal macros and eight for the input buffer. Loading of B_{OUT6} is 80 pF, BIOT12 and B3STA12 are 120 pF.

Derating Factors: $\mathbf{t_P = K_P \times K_t \times K_V \times t_{NOMINAL}}$

Process												
Process		Best			Nominal			Worst				
K_P		0.82			1.00			1.28				
Ambient Temperature °C												
T_A	–55	–40		0	25		70	85		125		
K_T	0.74	0.79		0.92	1.00		1.15	1.20		1.32		
Supply Voltage												
V_{DD}	2.7	3	3.13	3.3	3.47	3.6	4	4.5	4.75	5	5.25	5.5
K_V	1.89	1.66	1.58	1.49	1.41	1.35	1.23	1.1	1.05	1	0.96	0.93

External Timing Characteristics

(Over the Operating Range)

These timing parameters are provided for information only. Actual pin-to-pin timing characteristics guaranteed for ULCs are determined by the original FPGA or PLD data sheet plus any specific parameters that are agreed to separately by MHS.

Parameter	Symbol	Base Part	SSO	Min	Max		Unit
					Typ	Max	
Propagation Time	t_{PD}	UG00–02			5.0	7.5	ns
		UG04–UG09			6.0	9.0	
		UG14–UG20			7.0	10.5	
		UG33–UG90			8.5	13.0	
		UG120–UG200			9.5	14.5	
Clock Delay Time	t_{CO}	UG00–02	32		6.5	10.0	
		UG04–UG09	50		7.5	11.5	
		UG14–UG20	100		8.5	13.0	
		UG33–UG90	220		10.0	15.0	
		UG120–UG200	300		11.0	16.5	
Hold Time	t_H			0.0			
Output Enable Time	t_{EN}	UG00–02	32		6.5	10.0	
		UG04–UG09	50		7.5	11.5	
		UG14–UG20	100		8.5	13.0	
		UG33–UG90	220		10.0	15.0	
		UG120–UG200	300		11.0	16.5	

Power Consumption

Static Power Consumption for UC Series ULCs

There are three main factors to consider:

1. Leakage in the core:

   $P_{LC} = V_{DD} * I_{CCSB} *$ number of used gates

2. Leakage in inputs and tri-stated outputs:

   $P_{LIO} = V_{DD} * (I_{IX} * N + I_{OZ} * M)$

   where: N = number of inputs

   M = number of tri-stated outputs

   Care must be taken to include the appropriate figure for pins with pull-ups or pull-downs. In practice, the static consumption calculation is typically done to determine the standby current of a device; in this case only those pins sourcing current should be included, i.e. where V_{IN} or $V_{OUT} = V_{DD}$.

3. Dc power dissipation in driving I/O buffers due to resistive loads:

   In practice, the static consumption calculation is typically done to determine the standby current of a device, and under circumstances where all of the outputs are tri-stated or in input mode. So this term is zero.

   Global formula for static consumption:

   $P_{SB} = P_{LC} + P_{LIO}$

Dynamic Power Consumption for UC Series ULCs

There are four main factors to consider:

1. Static power dissipation is negligible compared to dynamic and can be ignored.

2. Dc power dissipation in I/O buffers due to resistive loads:

   P_1 (mW) = $V_{OL} * \Sigma_n (D_{Ln} * I_{OLn}) + (V_{DD} - V_{OH}) * \Sigma_n (D_{Hn} * I_{OHn})$

   where: Σ_n is a summation over all of the outputs and I/Os.

   I_{OLn} and I_{OHn} are the appropriate values for driver n

   D_{Ln} = percentage of time n is being driven to V_{OL}

   D_{Hn} = percentage of time n is being driven to V_{OH}

   It is difficult to obtain an exact value for this factor, since it is determined primarily by external system parameters. However, in practice this can be simplified to one of two cases where the device is either driving CMOS loads or driving TTL loads. CMOS loads can be approximated as purely capacitive loads, allowing this term to be treated as zero. TTL loads source significant current in the low state, but not the high state, allowing the second summation to be ignored. If a 50% duty cycle is assumed for dynamic outputs driving TTL loads, this can be approximated as:

   P_1 (mW) = $V_{OL} * (\Sigma_n * I_{OLn}/2 + \Sigma_m * I_{OLm})$ (TTL loads)

   where n are dynamic outputs and m are static low outputs.

3. Dynamic power dissipation for the internal gates:

   P_2 (mW) = $V_{DD} * I_{DDOP} * \Sigma_g (N_f * f_g)/1000$

   where: N_f = number of gates toggling at frequency f_g

   f_g = clock frequency of internal logic in MHz

   Note: If the actual toggle rates are not known, a rule of thumb is to assume that the average used gate is toggling at one half of the input clock frequency.

4. Dynamic power dissipation in the outputs:

   P_3 (mW) = $V_{DD}^2 * \Sigma_n f_n * (C_{OUT} + C_n)/1000$

   where: f_n = clocking frequency in MHz of output n

   C_n = output load capacitance in pF of output n

   C_{OUT} = output capacitance from DC Characteristics

   Global formula for dynamic consumption:

   $P = P_1 + P_2 + P_3$

Example:

Static calculation

A 100-pin ULC with 3000 used gates, 10 inputs, 20 I/Os in input mode, 40 outputs all tri-stated. No pull-ups or pull-downs. Half of the pins are at V_{DD}, half at V_{SS}. Input clock is not toggling. For this example only the current calculation is desired, so the V_{DD} term in the equations is dropped.

$P_{LC} = 1 * 3000 = 3$ mA

$P_{LIO} = ((10 + 20) * 5 + 40 * 5)/2 = 105$ mA

$P_{SB} = 3 + 105 = 108$ mA

Dynamic Calculation

We take a 16-bit resettable ripple counter which is approximately 100 gates, operating at a clock frequency of 33 MHz, which gives an average clock frequency of 33 MHz/16 for each bit and each output. There are no static outputs on this device. Operation is at 5 V, and 6-mA outputs are used and loaded at 25 pF. The output buffers are driving CMOS loads.

$P_1 = 0$

$P_2 = 5 * 0.5 * 100 * 33/16/1000 = 0.5$ mW

$P_3 = 5^2 * 16 * 33/16 * (25 + 2)/1000 = 22$ mW

$P = 0 + 0.5 + 22 = 22.5$ mW

Typical ULC Test Conditions

For ac specification purposes, an improved output loading scheme has been defined for MHS high-drive (24 mA), high-speed ULC devices. The schematic below (Figure 1) describes the typical conditions for testing these ULC devices, using the standard loading scheme commonly available on high-end ATE.

Compared to a no-load condition, this provides the following advantages:

- Output load is more representative of “real life” conditions during transitions.
- Transient energy is absorbed at the end of the line to prevent reflections which would lead to inaccurate ATE measurements.

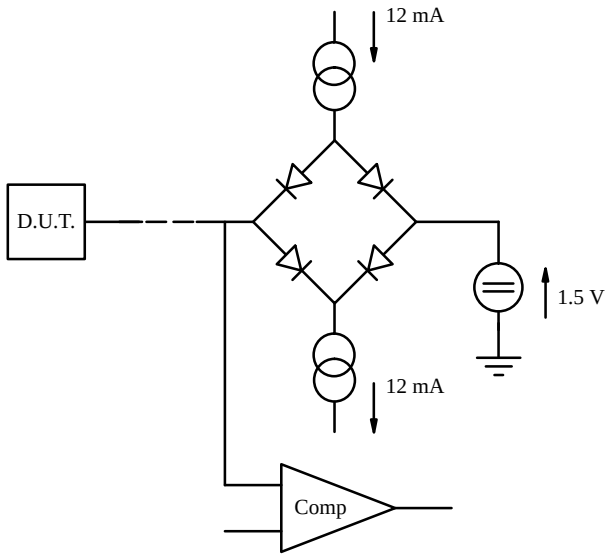

Figure 1. Typical ULC Test Conditions

ULC™ Ordering Information

Prior to conversion, ULCs are referred to by a generic ULC part number and separate package designation plus an optional temperature range formed as follows:

ULC/ *base PLD or FPGA* *pins-package*

where *base PLD or FPGA* refers to 22 V, 10 or EPM7128 or XC3030

Example:
ULC part number for XC3030A-5PL84C would be: ULC/XC3030, 84-PLCC

After conversion, a specific ULC code is ordered as follows:

UC 12 – PQS 160 – MZZ

ULC Series

- **UC** — 0.85-mm, 2-metal CMOS
- **UD** — 0.8-mm, 1-metal CMOS
- **UG** — 0.8-mm, 2- or 3-metal CMOS

Base Matrix

- **UC** — 04, 08, 2, 5, 8, 10, 12, 22, 29, 35, 50, 66
- **UD** — 02, 03, 09, 10, 14, 16, 27
- **UG** — 00, 01, 02, 04, 09, 14, 20, 33, 42, 52, 70, 90, 120, 140, 200

Package

- **PD** — Plastic Dual-In-Line Package (PDIP)
- **SD** — Plastic Skinny Dual-In-Line Package (SDIP)
- **TQ** — Plastic Thin Quad Flatpack—1.4 mm (TQFP)
- **VQ** — Plastic Very-Thin Quad Flatpack—1.0 mm (VQFP)
- **BQ** — Plastic Bumpered Quad Flatpack (BQFP)
- **PL** — Plastic J-Lead Chip Carrier (PLCC)
- **PQS** — Plastic Quad Flatpack with Short Leads (PQFP)
- **PQL** — Plastic Quad Flatpack with Long Leads (PQFP)
- **PP** — Plastic Pin-Grid Array (PPGA)
- **RS** — Plastic Small Outline Package 300-mil (SOIC)
- **SS** — Plastic Small Outline Package 150-mil (SOIC)
- **CD** — Ceramic Dual-In-Line (CDIP)
- **CL** — Ceramic Leadless Chip Carrier (CLCC)
- **CQ** — Ceramic Quad Flatpack (CQFP)
- **CP** — Ceramic Pin-Grid Array (CPGA)
- **CJ** — Ceramic J-Lead Chip Carrier (CLCCJ)

Pin Count
Number of Pins

Pattern
Unique Customer Pattern Code